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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/554,970	02/05/2007	Wolfgang Hoess	14603-016US1 P2003,0256 U	1058

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EXAMINER	
POOS, JOHN W	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
03/02/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/554,970	HOESS, WOLFGANG	
	Examiner	Art Unit	
	JOHN W. POOS	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2009*.

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-14* is/are allowed.

6)☒ Claim(s) *1,5-7,15* is/are rejected.

7)☒ Claim(s) *2-4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Kang et al. (US 7,215,170).

In regard to Claim 1 (as taught in Figure 3):

A flip-flop circuit arrangement, comprising:

input terminals (CLK and CLK inverse input terminals) to provide a differential clock signal (CLK and CLK inverse);

output terminals (Q and Q inverse output terminals) to provide a differential output signal (Q and Q inverse);

differential amplifiers (N4, N5 and N10, N11), each of the differential amplifiers comprising at least two transistors (N4, N5 and N10, N11), the transistors comprising collectors, each collector being part of one of plural series circuits containing a resistor (R1-R6), the series circuits being positioned between a power supply potential terminal (Vcc) and a first shared emitter node (common emitters of N16, N4, N5, and N6) and/or a second shared emitter node (common emitters of N18, N10, N11, and N12), sets of the collectors being interconnected to form a D flip-flop structure (N16, N4, N5, N6, N18, N10, N11, and N12 collectors connected through N7 and N8, and Figure 3 depicts a flip-flop circuit, see Brief Description of Figure 3 Column 7: lines 53-55), the output terminals being at an output of at least one differential amplifier (outputs Q and Q inverse connected to N10 and N11);

a first current source (C2) to connect the first shared emitter node (common emitters of N16, N4, N5, and N6) to a reference potential terminal (GND);

a second current source (C4) to connect the second shared emitter node (common emitters of N18, N10, N11, and N12) to the reference potential terminal (GND);

a first switch (N6) directly connected to the power supply potential terminal (Vcc) and directly connected to the first shared emitter node (common emitters of N16, N4, N5, and N6), the first switch having first control terminal that comprises part of the input terminals (N6 base connected to CLK inverse);

a second switch (N12) directly connected to the supply potential terminal (Vcc) and directly connected to the second shared emitter node (common emitters of N18, N10, N11, and

N12), the second switch having a second control terminal that comprises part of the input (N12 base connected to CLK).

In regard to Claim 6:

The flip-flop circuit of claim 1, wherein the flip-flop circuit is implemented in emitter-coupled logic circuit technology. (Column 4: lines 30-33)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (US 7,215,170), in view of Tung et al. (US 6,559,693).

In regard to Claim 5:

All of the claim limitations have been discussed with respect to Claim 1 above, except for wherein the first current source and the second current source each comprise a transistor in implemented using metal oxide semiconductor circuit technology.

Tung (693) teaches, in Figure 1, wherein the first current source and the second current source each comprise a transistor in implemented using metal oxide semiconductor circuit technology (MC 1, MC2 and Tung Column 3: lines 12-14). It would have been obvious to one skilled in the art at the time of the invention to use MOSFET technology for the current sources, in order to achieve low operating power consumption and low supply voltage requirements (Tung Column 1: lines 37-38).

7. Claims 7 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et al. (US 7,215,170).

In regard to Claim 7:

All of the claim limitations have been discussed with respect to Claim 1 above, except for a shift register comprising the flip-flop circuit of claim 1. The examiner takes Official Notice that it is old and notoriously well known to form a shift register using flip-flop circuits. Therefore it would have been obvious to one skilled in the art at the time of the invention to use the flip-flop taught by Kang '170 in a shift register in order to obtain the benefits/advantages taught by Kang, i.e. providing SET/RESET capability to a flip-flop (Column 4: lines 22-23).

In regard to Claim 15:

All of the claim limitations have been discussed with respect to Claim 9 above, except for a shift register comprising the flip-flop circuit of claim 9. The examiner takes Official Notice that it is old and notoriously well known to form a shift register using flip-flop circuits. It would have been obvious to one skilled in the art at the time of the invention to use the flip-flop taught by Kang '170 in a shift register in order to obtain the benefits/advantages taught by Kang '170, i.e. providing SET/RESET capability to a flip-flop (Column 4: lines 22-23).

Allowable Subject Matter

8. Claims 9-14 are allowed.

9. Claims 2-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hayakawa (US 5,969,556) teaches that a shift register comprises a flip-flop circuit (Column 4: lines 20-23).

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN W. POOS whose telephone number is (571)270-5077. The examiner can normally be reached on M-F (alternating Fridays off), 8:00 a.m - 4:00 p.m E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth B Wells/
Primary Examiner, Art Unit 2816

/J. W. P./
Examiner, Art Unit 2816